results in the formation of a plurality of first spacer cavities or gaps **34**G adjacent the first sacrificial sidewall spacers **20**. However, in this embodiment, the parameters of the etching process **34** are controlled so as to intentionally recess the layer of insulating material **26**, i.e., to intentionally form recesses **26**A in the area **36**, as shown in FIG. **2**P. Thereafter, as shown in FIG. **2**Q, processing is continued as described above until it is time to form the low-k sidewall spacers **60** in the second spacer cavities **54**A adjacent the replacement gate structure **50**. Due to the formation of the recesses **26**A in the layer of insulating material **26**, illustrative voids **70** are formed within the sidewall spacers **60**. That is, the low-k material tends to fill the recesses **26**A first and then "pinch-off" as the remainder of the cavity **54**A is filled with low-k material, thereby resulting in the formation of the illustrative voids **70**. The size and configuration of the voids **70** may vary, but their presence within the low-k sidewall spacers **60** effectively reduces the overall k value of the low-k sidewall spacers. The size of the voids **70** may be determined, at least in part, based upon the size of the recesses **26**A formed in the layer of insulating material **26**.

[0045] The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

1.-**16**. (canceled)

17. A device, comprising:

a gate structure positioned above a semiconducting substrate, said gate structure comprising a gate insulation layer and a gate electrode, said gate insulation layer having two upstanding portions that are substantially vertically oriented relative to an upper surface of said substrate; and

a low-k sidewall spacer positioned adjacent each of said vertically oriented upstanding portions of said gate insulation layer.

18. The device of claim **17**, wherein said low-k sidewall spacer is comprised of a material having a k value of less than 7.

19. The device of claim **17**, wherein said low-k sidewall spacer is positioned adjacent and contacts each of said vertically oriented upstanding portions of said gate insulation layer.

20. The device of claim **17**, further comprising a void formed in said low-k sidewall spacer.

21. The device of claim **17**, further comprising a layer of insulating material positioned that is laterally spaced away from said gate structure, said layer of insulating material having a recess formed therein, wherein a portion of said low-k spacer material extends into said recess.

22. The device of claim **17**, wherein said gate insulation layer is comprised of a high-k insulating material and said gate electrode is comprised of at least one layer of metal.

23. A device, comprising:

a gate structure positioned above a semiconducting substrate, said gate structure comprising a gate insulation layer and a gate electrode, said gate insulation layer having two upstanding portions that are substantially vertically oriented relative to an upper surface of said substrate; and

a low-k sidewall spacer that is positioned adjacent to and contacts each of said vertically oriented upstanding portions of said gate insulation layer, wherein said low-k sidewall spacer is comprised of a material having a k value of less than 7.

24. The device of claim **23**, further comprising a void formed in said low-k sidewall spacer.

25. The device of claim **23**, further comprising a layer of insulating material that is laterally spaced away from said gate structure, said layer of insulating material having a recess formed therein, wherein a portion of said low-k spacer material extends into said recess.

26. The device of claim **25**, wherein said gate insulation layer is comprised of a high-k insulating material and said gate electrode is comprised of at least one layer of metal.

27. A device, comprising:

a gate structure positioned above a semiconducting substrate, said gate structure comprising a gate insulation layer, a high-k insulating material and a gate electrode comprised of at least one layer of metal, said gate insulation layer having two upstanding portions that are substantially vertically oriented relative to an upper surface of said substrate;

a low-k sidewall spacer that is positioned adjacent to and contacts each of said vertically oriented upstanding portions of said gate insulation layer, wherein said low-k sidewall spacer is comprised of a material having a k value of less than 7;

a void within said low-k sidewall spacer; and

a layer of insulating material that is laterally spaced away from said gate structure, said layer of insulating material having a recess formed therein, wherein a portion of said low-k spacer material extends into said recess.

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